7.3-GHz Dynamic Frequency Dividers Monolithically Integrated in a Standard Bipolar Technology

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Abstract—**Monolithic integrated microwave 1/2 and 1/8 frequency dividers were developed and fabricated in standard 2-μm bipolar technology. The circuits which operate from about 2 to 7.3 GHz are based on the principle of "regenerative frequency division." Assuming that the same technology is used, this principle makes it possible to double the upper frequency limit, compared to the most popular static master–slave D-flip-flop dividers. Furthermore, power consumption can be considerably reduced.**

I. Introduction

HIGH-SPEED MONOLITHIC integrated frequency dividers in silicon bipolar technology are usually realized by an ECL master–slave D-flip-flop (MS-D-FF) with the inverted output fed back to the data input. With this principle, frequencies up to about 9 and 10 GHz have been achieved by applying sophisticated self-aligning polysilicon processes together with 1-μm photolithography (resulting in an emitter stripe width of 0.35 μm) [1], [2]. Recently, it has been demonstrated that by careful circuit design, rather high frequencies, of 7 GHz [3] and 8 GHz [14], can also be achieved by using conservative 2-μm photolithography. However, self-aligning polysilicon processes were also required in this case.

In an earlier work [4], [5] the authors showed that by using the principle of "regenerative frequency division," described by Miller in 1939 [6], the maximum divisible frequency can be doubled compared to the MS-D-FF principle (same technology assumed) in addition to considerably smaller power consumption. These results were demonstrated in [4] and [5] by the development of a 5.3-GHz divide-by-two circuit applying rather conservative 2-μm technology without needing any polysilicon process. This device was the very first application of Miller's concept in a monolithic integrated circuit. The good results were achieved by modifying a proposal of Kasperkovitz [7].

Miller's divider principle has also been applied in GaAs MESFET circuits. For example, Rauscher achieved an input frequency of 16 GHz with a single discrete transistor [15], and Ohira *et al.* achieved 14 GHz with a three-chip solution [16]. In both cases, the bandwidth is relatively small (600 MHz and 800 MHz, respectively) compared to the monolithic integrated bipolar divider presented.

In this paper it will be shown that regenerative frequency division in monolithic integrated circuits is not restricted to 1/2 dividers, but can also be applied to, e.g., three-stage 1/8 dividers. This is very important for realizing high-frequency low-power dividers with large divider ratios, as will be shown in the following example. Let us assume a 6-GHz divider with 250 mW power consumption and a large divider ratio, which is to be realized using a modern standard bipolar production technology. Of course, the first divide-by-two stage must be a regenerative frequency divider (RFD). If the second 3-GHz stage is to be realized as a MS-D-FF divider, its power consumption will be considerably higher than that of the first 6-GHz stage and will exceed the given power limit. Therefore, frequency division should be carried out by RFD's down to a frequency which can also be divided by *low-power* MS-D-FF dividers. In our example this may be a frequency below 1 GHz, which requires an 1/8 RFD.

In the next section the principle of regenerative frequency division is briefly recapitulated together with the basic divide-by-two cell used. This is followed by a discussion of the design and realization of 1/2 and 1/8 dividers. The final presentation of experimental results demonstrates that, with this principle, reliable operation up to 7.3 GHz can be achieved by applying rather conservative bipolar technology. More detailed information about the dividers presented in this paper as well as a previously unavailable simple large-signal theory related to stability ranges will be given in [13].

II. Principle of Operation and Basic Divide-by-Two Cell

The block diagram of a 1/2 RFD is shown in Fig. 1 (cf. [6]). One port of the mixer is fed with the input signal of the divider circuit, which has frequency f, whereas the other port is fed with the output signal of frequency $f/2$. The output signal of the mixer contains frequency $f/2$ and, in the case of a well-balanced mixer, only its odd harmonics $3f/2$, $5f/2$, etc. These harmonics are filtered out and the signal of frequency $f/2$ is amplified to com-

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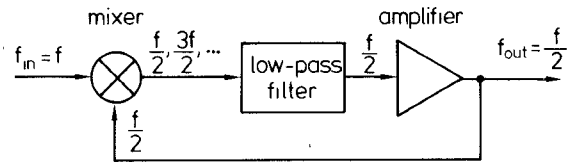

Fig. 1. Principle of regenerative frequency division [6].

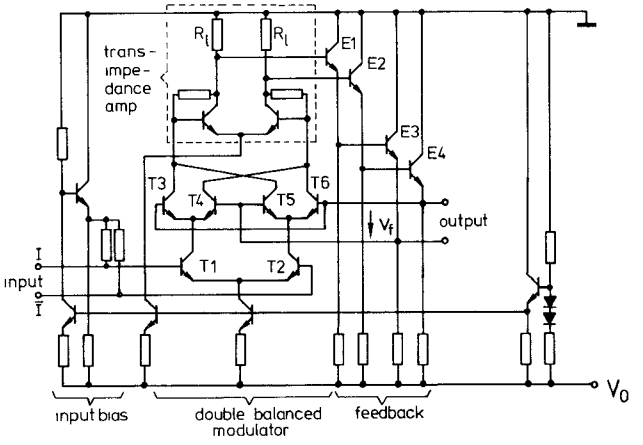

Fig. 2. Circuit diagram of the divide-by-two cell (including bias voltage generators). The input bias is only required for the first stage.

pensate for conversion loss and, finally, is fed back to the mixer.

The maximum input frequency f_{max} of this circuit concept is mainly determined by the upper cutoff frequency of the loop (limited by both the mixer and the amplifier) rather than by the loop delay.[1] It was shown by simulation and later verified by experiment that because of this, f_{max} can be doubled compared to the MS-D-FF principle, where f_{max} is limited by the two gate delays in the loop. However, regenerative frequency division has a considerably higher minimum frequency f_{min} because the harmonic $3f/2$ can no longer be suppressed if f falls well below $f_{max}/3$ (cf. Section IV). But for many applications this is not a real disadvantage of the RFD. Furthermore, it should be mentioned that, in contrast to the MS-D-FF divider, the RFD shows no self-oscillation (in the absence of an input signal) so that no measures have to be taken to avoid such a disadvantage.

Fig. 2 shows the circuit diagram used for the basic divide-by-two cell. The mixer is realized by a double-balanced modulator (T1–T6). The input voltage drives the lower differential transistor pair (T1–T2) while the feedback voltage v_f, which equals the output voltage, is applied to the upper stage of the modulator. In principle, the modulator in Fig. 2 itself already contains all the functions of the block diagram in Fig. 1, even if, as in [7], its output is directly loaded by the resistors R_l. However, much better results (with regard to maximum frequency, safe broad-band operation, and high input sensitivity) can be achieved if the simple transimpedance amplifier shown in Fig. 2 is inserted at the modulator output [8]. This stage, together with the feedback emitter-followers (E1–E4), increases the desired mismatching within the loop (demanded by the broad-band amplifier theory) and, moreover, further improves the frequency response of the loop. The emitter-followers are also needed for level shifting. Note that an extra low-pass filter (cf. Fig. 1) is not required in the loop because of the well-designed low-pass characteristic of the amplifier. This fact simplifies monolithic integration considerably.

The input bias network shown in Fig. 2 allows ac coupling of the input signal without needing any additional external circuitry. Of course, it is only required in the first stage of the divider.

III. Circuit Design and Realization

Both the 1/2 and 1/8 divider are placed on the same chip and are personalized by the second metallization level only. The 1/2 divider consists only of the stage in Fig. 2 and a 50-Ω output buffer with open collector outputs. Since this circuit was already presented in [4] and [5], we will now confine ourselves to the more interesting 1/8 divider.

Fig. 3 shows the block diagram. The first divider stage is identical with that of the 1/2 divider already discussed (Fig. 2). The circuit diagrams of the second and third stages are nearly equal to that of the first stage, but resistances and transistor sizes differ considerably. The designer has the very important task of adjusting the frequency ranges of the different stages in such a manner that the total frequency range is not much smaller than that of the first stage alone. This means that the second stage has to be slowed down by a factor of two and the third stage by a factor of four compared to the first stage. To achieve this, the current in the second and especially in the third stage has to be drastically reduced and the resistance ratios must be carefully chosen. For later fine adjustment, internal p-n junction capacitances are provided in the second and third stage, which allow the internal time constants to be changed by external resistors changing the voltage across the junction. However, because of accurate design, this measure was not needed here.

As a consequence of the low currents in the third stage, it is not possible to drive a 50-Ω line without using an appropriate output buffer. A buffer circuit well suited for this task with sufficiently high gain is shown in Fig. 4 (for discussion of such an amplifier stage, cf. [9]). In addition to impedance transformation, it has to amplify the output signal of the third stage, which may be considerably decreased in the region of the upper frequency limit. In contrast to a simple ohmic loading of the transistor pair T1–T2, the transimpedance stage (T3–T4) increases both voltage gain and bandwidth (due to mismatching) at even lower power consumption.

Because of the lower output frequency of the 1/8 divider, emitter followers are used at the output, which cannot be recommended for the output buffer of the 1/2

[1] However, too large a loop delay may cause unstable operation regions between f_{max} and the minimum input frequency f_{min}, thus reducing the usable frequency range.

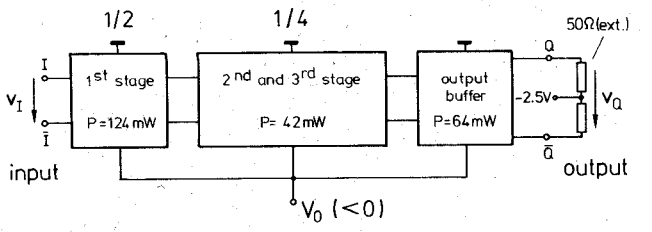

Fig. 3. Block diagram of the 1/8 divider including output buffer. The values of power consumption belong to a supply voltage $V_0 = -5$ V. The differential output voltage swing is about 1 V_{p-p}.

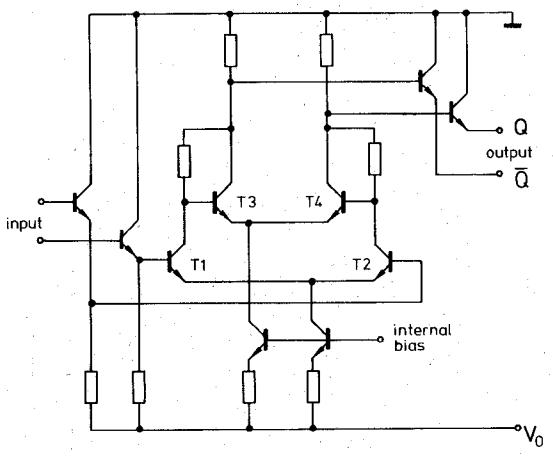

Fig. 4. Output buffer of the 1/8 divider. The emitter-follower outputs are able to drive matched 50-Ω transmission lines.

divider. Note that the power-consuming buffer stage is not required if the divider output drives further divider stages instead of 50-Ω transmission lines.

The aim of the design was to achieve maximum operating speed at low power consumption and stable operation in a large frequency range (i.e., optimum adjustment of the different divider stages). Therefore, a careful design was required, which included optimization of internal currents and voltage swings as well as individual optimization of all transistors in the circuit (e.g. [10]).

The numerous network simulations necessary for optimization were mainly carried out with a special analog computer developed at our institute some years ago [11]. Compared to conventional digital-computer simulation, this method allows the operating frequency and voltage ranges to be determined very quickly, thus considerably reducing optimization time and costs.

It should be pointed out that the maximum input frequency of this circuit is nearly as high as the transit frequency of the transistors. As a consequence, for accurate simulation two-transistor models should be used which take into account the reduction of the effective internal base spreading resistance at high frequencies [12]. Such models were implemented in both the analog simulator and the network analysis program SPICE 2. As a further consequence of the high input frequency, the influence of parasitic elements such as bond inductances and pad capacitances has to be carefully simulated. These elements may considerably influence the operating range, especially in the region of the upper frequency limit.

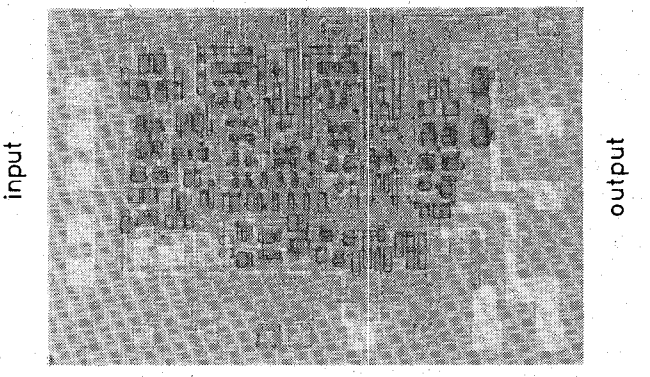

Fig. 5. Chip with the 1/8 divider (1.2 mm × 0.8 mm).

The circuit design was based on the bipolar technology mentioned below, assuming a standard power supply voltage[2] of −5 V and a maximum junction temperature of 90°C. Furthermore, worst-case conditions were carefully considered, such as design tolerances, fabrication spread, and tolerance of the supply voltage. The power consumptions of the different stages (including the corresponding contribution of the internal bias voltage network) are given in Fig. 3. The total power consumption of the 1/8 divider including the buffer stage is 230 mW; without the buffer it is 166 mW. The swing of the differential output voltage v_Q is about 2×500 mV $= 1$ V_{p-p}.

As shown in the next section, the frequency divider can be operated up to 7.3 GHz. This means an upper input frequency limit of the 1/4 divider (consisting of the second and third stage) of at least 3.65 GHz at a power consumption of only 42 mW. This result again demonstrates the suitability of regenerative frequency division for low-power microwave dividers. As shown by network simulations, the power consumption of the first stage can also be considerably reduced if a reduction of the upper frequency limit by only a few hundred MHz is acceptable.

The circuits are fabricated using standard bipolar technology with rather conservative 2-μm photolithography. This technology, available at our institute, has already been briefly described elsewhere (e.g. [10]). It is similar to that used in [4] and [5] but the transit frequency of transistors (at optimum collector current density) of about 8 GHz ($V_{CE} = 1$ V) is somewhat higher. No super self-aligning polysilicon processes with polysilicon emitter technology are applied.

Fig. 5 shows the chip, wired for the 1/8 divider including buffer stage and bias voltage generator.

IV. Experimental Results

For measurement purposes the chip was mounted directly on a ceramic substrate with its 50-Ω signal lines and blocking capacitors.

Fig. 6 shows the input voltage range of the 1/8 divider versus frequency in which stable operation is ensured. The

[2]As shown in Section IV, the operating speed can be increased if the circuit is measured at a higher supply voltage V_0, e.g. −5.5 V. An even greater improvement is achievable if the circuit is already designed for a higher V_0.

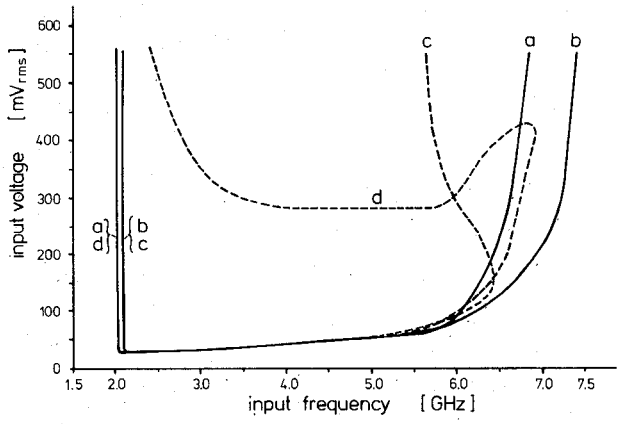

Fig. 6. Range of stable operation for the 1/8 divider (r.m.s. value of the differential input voltage versus frequency). The different curves, defined in the text, can be extended up to the measuring limit of 1 V_{rms}.

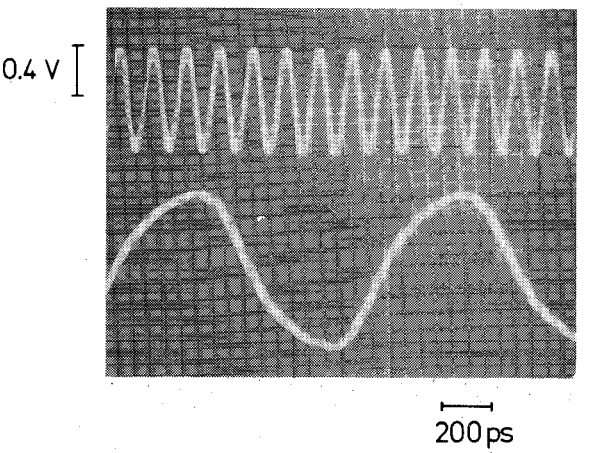

Fig. 7. Input (top) and output (bottom) signals of the 1/8 divider at $f = 7.2$ GHz (case b).

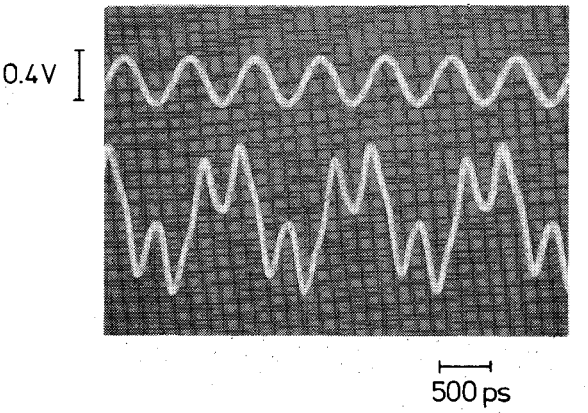

Fig. 8. Input (top) and output (bottom) signals of the 1/2 divider in the region of its lower frequency limit ($f = 1.5$ GHz).

input voltage is defined as the *effective* (r.m.s) value of the differential voltage of the driving RF generator (loaded by 50 Ω rather than by the input of the circuit). Four different cases are presented:

a) differential-mode input signal (i.e., the signals at I and $\bar{I}$ are shifted in phase by π against each other), $V_0 = -5$ V;
b) like a) but $V_0 = -5.5$ V;
c) single-ended input signal at I ($\bar{I}$ grounded via 50 Ω), $V_0 = -5.5$ V;
d) single-ended input signal at $\bar{I}$ (I grounded via 25 Ω), $V_0 = -5.5$ V.

The curves demonstrate the high input sensitivity of the divider over a large frequency range. In all cases the lower limit of the operating frequency f_{min} is about 2 GHz; moreover, there is no marked difference in the minimum input voltage up to about 6 GHz. For differential-mode input signals, the maximum frequency f_{max} is 6.8 GHz at $V_0 = -5$ V (curve a) and 7.4 GHz at $V_0 = -5.5$ V (curve b).[3] Up to an input voltage of at least 1 V_{rms} (limited by the driving RF generator), the divider shows stable operation over the total frequency range.

For single-ended signals at input I (curve c), f_{max} is reduced to about 6.4 GHz ($V_0 = -5.5$ V). Furthermore, at high frequencies the maximum permissible input voltage is reduced compared to the differential mode. For single-ended signals at input $\bar{I}$ (curve d), $f_{max} \approx 6.8$ GHz was achieved ($V_0 = -5.5$ V). However, the maximum permissible input voltage is then reduced at medium and low frequencies. All these experimental results were predicted from preceding circuit simulations.

Fig. 7 shows the differential input voltage and the differential output voltage of the 1/8 divider at $f = 7.2$ GHz and $V_0 = -5.5$ V for differential-mode input signals with the output loaded by 50 Ω.

Similar results were achieved with the 1/2 divider. The slightly smaller value of the lower frequency limit ($f_{min} \approx$ 1.5 GHz for case a) shows that the lower frequency limit of the 1/8 divider is caused by the second or third stage.[4] Fig. 8 shows the input and output waveforms of the 1/2 divider in the region of the lower frequency limit. It can be seen that the third harmonic ($3f/2$) of the divided frequency ($f/2$) can no longer be suppressed by the low-pass characteristic of the closed loop in Fig. 1. This is because $3f/2$ is smaller than the cutoff frequency of this loop, which is about $f_{max}/2$.

The phase noise performance of the 1/2 divider was measured at 4 GHz input frequency by staff members of Wandel & Goltermann (Eningen, W. Germany) using a phase detector method. At 10 kHz offset from the carrier and above, the (single-sideband) phase-noise-to-signal ratio was about −140 dBc/Hz, a rather low value.

V. Conclusions

The circuits developed belong to the fastest monolithic integrated frequency dividers fabricated in silicon technology in spite of the fact that rather conservative technology

[3] Power consumption is increased by 24 percent if V_0 is changed from −5 V to −5.5 V.

[4] As mentioned in Section III, this frequency limit can be reduced by increasing internal junction capacitances via external resistors. This adjustment was not applied for the measurements presented in this section.

was used. The results demonstrate the advantages of regenerative frequency division compared to the MS-D-FF principle used in customary monolithic integrated frequency dividers. The maximum input frequency is about twice as high and the power consumption is considerably lower. This means that by employing modern silicon bipolar technologies with self-aligning polysilicon processes, low-power frequency dividers operating above 15 GHz can be fabricated.

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